

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jie Liang	Docket No.:	TI-36793
Serial No.:	10/724,494	Art Unit:	2618
Filed:	11/28/2003	Examiner:	LEE, John J.
For:	RECEIVER DIRECTED POWER MANAGEMENT FOR WLAN RECEIVER	Confirm. No.:	1020

**DECLARATION OF PRIOR INVENTION IN THE UNITED STATES
TO OVERCOME CITED US PATENT APPLICATION (37 C.F.R. § 1.131)**

Mail Stop Non-Fee Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22131-1450

Dear Sir:

1. This declaration is to establish conception of the invention in the above identified application in the United States at a date prior to September 30, 2003, which is the first effective date of the cited U.S. patent publication to Simpson et al. (US 2005/0128988 A1—filed on September 10, 2004), which was cited by the Examiner and parent application published as (US 2005/068928 A1—filed on September 30, 2003), and diligence in filing a patent application therefor.

2. The individual making this declaration Jie Liang is the sole inventor of US Patent Serial Number 10/734,494.

3. The filing date of US Patent Serial Number 10/734,494, filed on November 28, 2003. Which is before the filing date US 2005/0128988 A1 cited by Examiner.

4. To establish the date of conception of the invention of this application and diligence in reducing to practice, a true copy of a portion of the disclosure form submitted to the Patent Department, Texas Instruments Incorporated and assigned docket no. TI-36793 is submitted as evidence (Exhibit A). The disclosure was date-stamped July 18, 2003. This disclosure was made

prior to the September 30, 2003 filing date of the parent US 2005/068928 of the patent application publication US 2005/0128988 cited by Examiner.

5. This declaration is submitted prior to final rejection.

6. As a person signing below:

I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Jie Liang

Date:



TI INVENTION / INNOVATION DISCLOSURE

TI-36993

SEND COMPLETED FORM TO: TI CORPORATE PATENTS
ATTN: Tina Smith
E-Mail: tina-smith@ti.com
FAX: (972) 917-4418
Mail Station M/S 3999
PC Drop PPC-B

HELPLINE: Warren Franz
E-Mail: w-franz@ti.com
PHONE: (972) 917-5271
FAX: (972) 917-4418

If you are employed by a TI subsidiary company, send this form to your site coordinator.

To prepare your invention disclosure, follow the step-by-step directions on the form that follows. Type or print answers to the questions in the spaces provided.

PLEASE PROVIDE ANSWERS TO ALL OF THE QUESTIONS
OTHERWISE THERE COULD BE DELAYS IN PROCESSING

If you already have an engineering spec, please send it with your invention disclosure. Computer documentation and drawings, marketing foils, notebook entries, paper manuscripts, articles, and any other material that you already have can be copied or sent electronically.

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#44045

Appendix A

PATENT DISCLOSURE FORM

DOCKET NO. TI-(to be filled in by Patent Activity)

IF ELECTRONICALLY TRANSMITTED, PROCESSING OF YOUR DISCLOSURE CANNOT BE COMPLETED WITHOUT A FOLLOW-UP COPY SIGNED AND DATED BY ALL INVENTORS AND AT LEAST ONE WITNESS.

1. Please suggest a descriptive title for your invention:

Receiver Directed Power Management Architecture for Low Power WLAN Chipset Design

2. This invention supports strategy: (check 1 or more)

☐
☐
☐
☐
☐

DLP
Materials
Fab/Processes
Assembly/Test/Packaging
Other

DSPS

☒ Wireless
☐ Video
☐ Set Top
☐ Application Specific
☐ Remote/Access/Networking
☐ Emerging Markets
☐ Mixed Signal & Logic
☐ Mass Storage
☐ Other

3. What is the problem solved by your invention?

To reduce the power consumption of WLAN chipset.

4. What is your solution to the problem?

WLAN baseband uses a packet based protocol, which is bursty by design. The packet protocol includes preamble, header, and payload. Many processing tasks are active only during a portion of a packet data. We take advantages of this fact for power management.

5. When was your solution first conceptually or mentally complete?

Date: 05/2003

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6. What is the first tangible evidence of such completion?

Date: 07/2003

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7. What is different about your solution, compared with other solutions to the same problem?

Most of the WLAN chipset manage power at the top module (TX, RX, IDLE, SLEEP, etc). In this invention, we use the RX state information to control the CTS (clock tree) of the WLAN chip. This results in fine grain control of the power state and lower power consumption.

8. What are the advantages of your solution?

Lower Power.

9. What TI products, processes, projects or operations currently implement your invention?

In discussions with WLAN BU regarding implementation.

10. What is the date of the first implementation?

Date: N/A

11. What record exists to prove this date?

N/A

12. Is there any future implementation planned?

Yes ☐ No ☒

If so, please furnish the TI PART No. or project name

13. Has the invention been published or disclosed to anyone outside of TI?

Yes ☐ No ☒

When?

If planned - when? (Catalog, advertising, data book, application note, conference paper, magazine article, TI TJ, proposal document.)

Was there a nondisclosure agreement (NDA)?

Yes ☐ No ☐

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14. Has a TI product incorporating the invention been publicly introduced, quoted, sampled or shipped?

Yes ☐ No ☒

When? If planned—when?

15. Was the invention conceived or first implemented in the performance of a government contract or subcontract?

Yes ☐ No ☒

Contract #:

THE INVENTION DESCRIBED BY THIS DISCLOSURE IS SUBMITTED
PURSUANT TO MY EMPLOYMENT AGREEMENT WITH TEXAS INSTRUMENTS
INCORPORATED OR A TI SUBSIDIARY (SPECIFY):

Has this disclosure been previously sent to the Patent Department electronically (unsigned)?

Yes ☒ No ☐

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PLEASE PRINT ALL INVENTOR INFORMATION.

Inventor 1's Name: Jie Liang
(First, Middle, Last)

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(Street, City, State, Zip)

E-Mail Address: liang@ti.com

Employee #: 0212054

TI Division & Cost Center 003/05113

Phone #: 2144804105

Pager #:

Country of Citizenship: P.R.China

Inventor 1's Signature: _____

Date: 07/15/2003

Mail Station:

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PLEASE PRINT ALL INVENTOR INFORMATION.

Inventor 1's Name: Jie Liang
(First, Middle, Last)

Home Address: 2505 Frosted Green Ln, Plano, TX 75025
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E-Mail Address: liang@ti.com

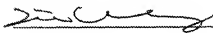
Employee #: 0212054

TI Division & Cost Center 003/05113

Phone #: 2144804105

Pager #:

Country of Citizenship: P.R.China

Inventor 1's Signature: 

Date: 07/15/2003

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Inventor 2's Name:

(First, Middle, Last)

Home Address:

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E-Mail Address:

Employee #:

TI Division & Cost Center

Phone #:

Pager #:

Country of Citizenship:

Inventor 2's Signature:

Date:

Mail Station

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Inventor 4's Name:

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E-Mail Address:

Employee #:

TI Division & Cost Center

Phone #:

Pager #:

Country of Citizenship:

Inventor 4's Signature:

Date:

Mail Station:

.....

This invention disclosure with any attachments was read and understood by me on

Markoff
Witness 1: _____

07/15/2003
Date _____

This invention disclosure with any attachments was read and understood by me on

Witness 2: _____

Date _____

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Receiver Directed Power Management (RDPM) for WLAN Receiver Design

Jie Liang
Communications Lab
DSPS R&D Center
Texas Instruments

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Motivation

- Low power is becoming an important factor for measuring WLAN chipsets:
 - Nokia
 - Motorola
- We look at fine granularity power control (clock gating) at the sub-packet processing level
- The clock zones are controlled by the Receiver state machine
- Once a module finishes its processing task, we shut down its clock

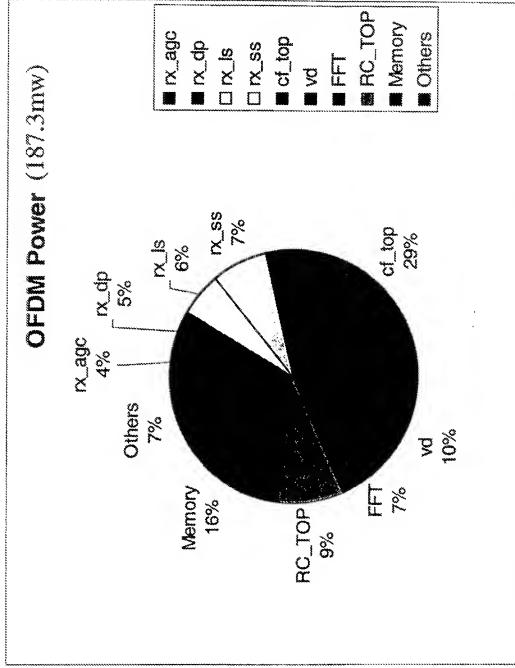
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1130 OFDM Receive Module: Power

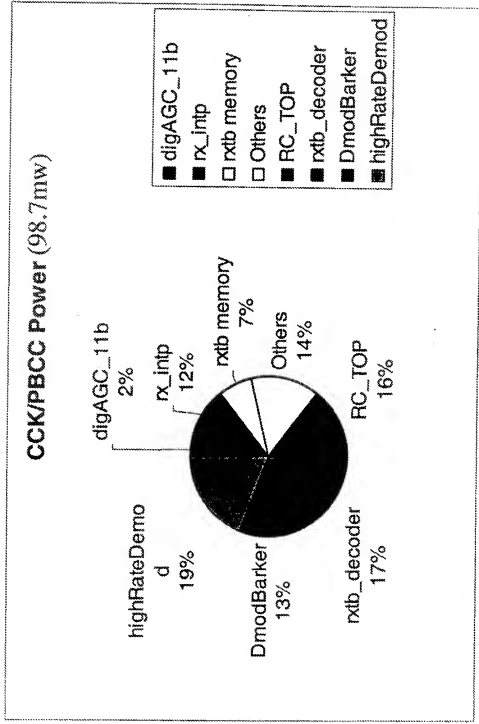


Note: power estimates using RFQ Power based on 1130 synthesis

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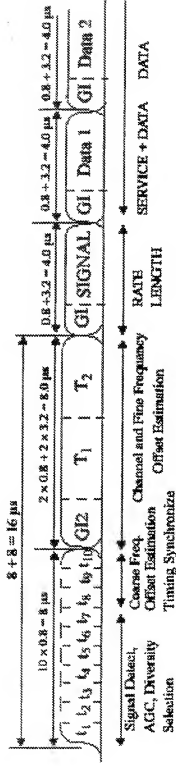
1130 CCK/PBCC Receive: Power



Note: power estimates using RFQ Power based on 1130 synthesis

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OFDM Processing Duty Cycle



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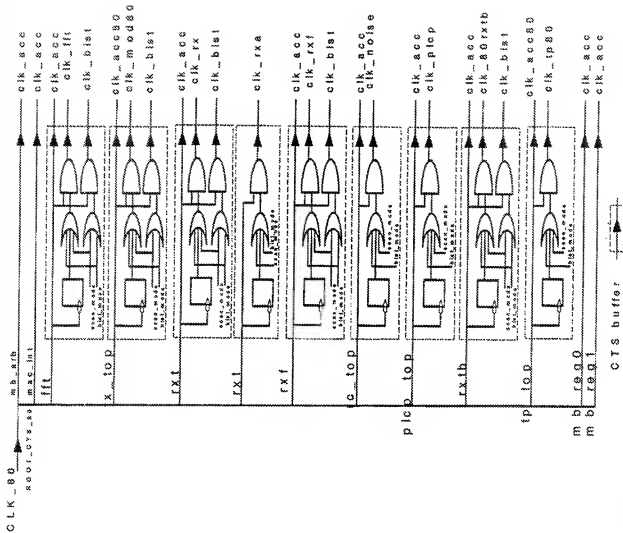
Many Processing Tasks occupy only a brief period:

- AGC
- Boundary and Packet Detection
- Short Sequence Processing
- Long Sequence Processing/Channel Estimation
- Radio Control Setting

⇒ These modules should be shut down based on the RX state machine state

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TNET1130 OFDM Clock Tree



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RDPM For Reducing Power for 1130

OFDM Baseband

- ☐ Add more clock zones to the previous Clock Tree and control them using RX states
- ☐ OFDM Rx Mode (payload portion):
 - RC_Top (RSSI/CCA portion) should be gated off after preamble
 - RX_AGC should be gated off after AGC settles
 - RX_DP (digAGC portion) should be gated off after AGC settles
 - Rx_ss should be off after short sequence processing
 - rx_ls should be off after long sequence processing
 - Only pilot processing and compensation should be active, and channel estimation should be off after long sequence

- ☐ Potential for power saving:

Current 187mw Target 106mw (based on RFQ Power estimates)

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Application in 1130LP OFDM Rx RTL Design

Module/clock Domain	Power	RTL Design in 1130	Design Change Proposal
Rc_top/ clk_80	16mw	Most modules use the system/MOAB clock and are not gated.	Gate Rc_top for the part not dealing with MOAB interface.
Rx_agc/ clk_rx	7mw	Gated by the common a/b/g rx clock enable signal. See module rx_reg. Essentially if the receiver is on, rx_agc is on all the time.	Gate the input clock clk_rx at the PHY state machine level, not at the top receiver module.
Rx_dp/ clk_rxa	9mw	digAGC and derotator are used by 11a. Clock sources are clk_rx and clk_rxa.	Should be able to turn off digAGC after AGC lock if the input clock was gated by state machine.
Rx_ss/ clk_rxa	14mw	Clock source: clk_rxa. Clk_rxa was gated by 11a receiver enable signal.	Should be controlled by 11a state machine, and turned off after packet and boundary detection
Rx_ls/ Clk_rxa	11mw	Clock source: clk_rx, clk_rxa, which were generated by rx_top module.	Should be controlled by 11a state machine, and turned off after long sequence processed
Cf_top/ Clk_rxf	56mw	Module clocked gated by signal rx_top_start (controlled by rx_ls module). rx_top_mode (high: estimation, low: compensation) is output of rx_ls module. Pilot processing and channel estimation from long sequence share the same computing resources	Both channel estimation and compensation model share the rx_top_start signal (high for enable). Even the estimation modules are active during compensation mode. Therefore, all modules are active during 11a rx. Separate estimation and compensation modules and should turn off estimation modules when only compensation and pilot processing is needed.
Saving	9+7+4+1 2+9+40= 81 mw		

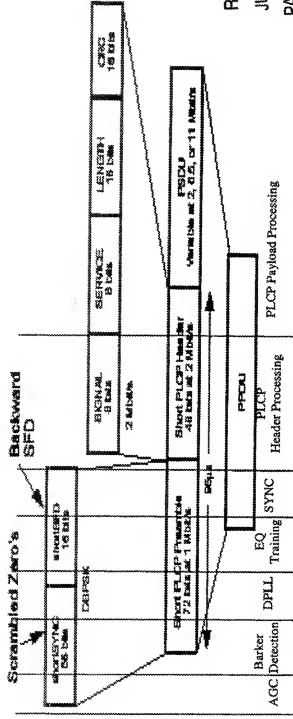
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CCK/PBCC Processing Duty Cycle



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Many Processing Tasks occupy only a brief period:

- AGC
 - Barker detection
 - Frequency offset correction
 - Channel estimation/DFE training
 - Radio Control Setting
- ⇒ These modules should be shut down based on the RX state machine state

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RDPM For Reducing Power for 1130 CCK Baseband

- ☐ Add more clock zone to the previous Clock Tree and control them using RX states
- ☐ 11b Rx Mode:
 - AGC should be off after AGC lock event
 - RC_top should be off after preamble
- ☐ Potential for power saving:
Current 93mw Target 84mw (based on RFQ Power estimates)

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Application in 1130LP CCK Rx RTL Design

Module	Power(mw)	RTL Design in 1130	Design Change Proposal
Rc_top	16	Most modules use the MOAB clock and are not gated. However, majority of the functions here do not change in Rx state.	Gate the Rc_top module also.
Total Power Saving from current estimate	9 mw		

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